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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,974	10/21/2003	Howard E. Rhodes	M4065.0650/P650	8113

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,974	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18,21-26 and 29-44* is/are rejected.

7)☒ Claim(s) *19,20,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-18 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. As to claim 11, Ackland et al., Figure 2, discloses a semiconductor device comprising a substrate and two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap of a few tens of nanometers (col. 3, lines 60-63), which may be in the range of from 10 nm to 90 nm.

As to claim 12, Ackland et al., Figure 2 (col. 3, lines 60-63), discloses that the gap is within the scope of being from 30 nm and 100 nm.

As to claim 13, Ackland et al., col. 3, line 35, discloses that the structure shown in Figure 2 is a double polysilicon structure.

As to claim 14, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager. Although Ackland et al. does not expressly disclose that the gate structure is part of a CCD imager, it is understood in the art that CCD imagers and CMOS imagers operate under the same charge-transfer mechanism. See, for example, applicants Background of the Invention, or Fossum et al., col. 1, lines 35-43).

As to claim 15, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager.

As to claim 16, Ackland et al., Figure 1, discloses that the CMOS imager illustrated has a 5T architecture.

As to claim 17, Ackland et al. discloses (col. 3, lines 38-39) that the transistor gates include a photogate (101) and a transfer gate (107).

As to claim 18, Ackland et al., Figure 3, discloses an embodiment with a photo gate (101) and transfer gate (108) (col. 5, lines 16-17) with a lightly doped region (112) between the two adjacent gate structures.

As to claim 21, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager. Although Ackland et al. does not expressly disclose that the gate structure is part of a CCD imager, it is understood in the art that CCD imagers and CMOS imagers operate under the same charge-transfer mechanism. See, for example, applicants Background of the Invention, or Fossum et al., col. 1, lines 35-43).

As to claim 22, Ackland et al. discloses (title and col. 5, lines 16-17) that the two gate structures (101) and (108) are transistor gates for a CMOS imager and are a photo gate and transfer gate, respectively.

As to claim 23, Ackland et al., Figure 3, discloses an embodiment with a photo gate (101) and transfer gate (108) (col. 5, lines 16-17) with a lightly doped region (112) between the two adjacent gate structures.

As to claims 24 and 25, although not explicitly stated by Ackland et al., it is conventional in the art that CMOS imager devices my be formed with p-channel or n-channel gates. See, for example, Lee et al., Figure 3d (col. 3, lines 9-11).

Claims 26 and 29-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. As to claim 26, Ackland et al., Figure 3, discloses a semiconductor device comprising a substrate, a plurality of conductive gates (101) and (108) formed over the substrate, and a lightly doped region (112) in the substrate between the two adjacent conductive gates (101) and (108).

As to claim 29, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager. Although Ackland et al. does not expressly disclose that the gate structure is part of a CCD imager, it is understood in the art that

CCD imagers and CMOS imagers operate under the same charge-transfer mechanism. See, for example, applicants Background of the Invention, or Fossum et al., col. 1, lines 35-43).

As to claim 30, Ackland et al. discloses (title and col. 5, lines 16-17) that the two gate structures (101) and (108) are transistor gates for a CMOS imager and are a photo gate and transfer gate, respectively.

As to claim 31, Ackland et al., Figure 3, discloses an embodiment with a photo gate (101) and transfer gate (108) (col. 5, lines 16-17) with a lightly doped region (112) between the two adjacent gate structures.

As to claims 32 and 33, although not explicitly stated by Ackland et al., it is conventional in the art that CMOS imager devices my be formed with p-channel or n-channel gates. See, for example, Lee et al., Figure 3d (col. 3, lines 9-11).

Claims 34-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. As to claim 34, Ackland et al., Figures 1 and 2, discloses an image processing apparatus comprising an image sensor (101) for detecting an image and outputting image signals corresponding to the detected image, and an image processor (120), (125), (130) and (135) for processing the image signals outputted from the image sensor, wherein the image sensor comprises a substrate and two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap of a few tens of nanometers (col. 3, lines 60-63), which may be in the range of from 10 nm to 90 nm.

As to claim 35, Ackland et al., Figure 2 (col. 3, lines 60-63), discloses that the gap is within the scope of being from 30 nm and 100 nm.

As to claim 36, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager. Although Ackland et al. does not expressly disclose that the gate structure is part of a CCD imager, it is understood in the art that CCD imagers and CMOS imagers operate under the same charge-transfer mechanism. See, for example, applicants Background of the Invention, or Fossum et al., col. 1, lines 35-43).

As to claim 37, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager.

As to claim 38, Ackland et al., Figure 3, discloses an embodiment with a photo gate (101) and transfer gate (108) (col. 5, lines 16-17) with a lightly doped region (112) between the two adjacent gate structures.

Claim 39 is rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. Ackland et al., Figures 1 and 2, discloses an image processing apparatus comprising an image sensor (101) for detecting an image and outputting image signals corresponding to the detected image, and an image processor (120), (125), (130) and (135) for processing the image signals outputted from the image sensor, wherein the image sensor comprises a substrate, a plurality of conductive gates (101) and (108) formed over the substrate, and a lightly doped region (112) in the substrate between the two adjacent conductive gates (101) and (108).

Claims 40-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. As to claim 40, Ackland et al., Figures 1 and 2, discloses a processing system comprising a processor for receiving and processing image data (35), and an image data generator (101), (107) for supplying image data to the processor, the image data generator comprising an image sensor for obtaining an image and outputting an image signal (35), an image processor (120), (125), (130) and (135) for processing the image signal and a controller (190) for controlling the image sensor and the image processor, wherein the image sensor comprises a substrate and two gate structures formed in a single layer on said substrate, said gate structures being spaced apart by a gap of a few tens of nanometers (col. 3, lines 60-63), which may be in the range of from 10 nm to 90 nm.

As to claim 41, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager. Although Ackland et al. does not expressly disclose that the gate structure is part of a CCD imager, it is understood in the art that CCD imagers and CMOS imagers operate under the same charge-transfer mechanism. See, for example, applicants Background of the Invention, or Fossum et al., col. 1, lines 35-43).

As to claim 42, Ackland et al. discloses (col. 2, lines 43-47) that the gate structure shown in Figure 2 is in a CMOS active pixel, which is within the scope of being an imager.

As to claim 43, Ackland et al., Figure 3, discloses an embodiment with a photo gate (101) and transfer gate (108) (col. 5, lines 16-17) with a lightly doped region (112) between the two adjacent gate structures.

Claim 44 is rejected under 35 U.S.C. 102(b) as being anticipated by Ackland et al.. Ackland et al., Figures 1 and 2, discloses a processing system comprising a processor for receiving and processing image data (35), and an image data generator (101), (107) for supplying image data to the processor, the image data generator comprising an image sensor for obtaining an image and outputting an image signal (35), an image processor (120), (125), (130) and (135) for processing the image signal and a controller (190) for controlling the image sensor and the image processor, wherein the image sensor comprises a substrate, a plurality of conductive gates (101) and (108) formed over the substrate, and a lightly doped region (112) in the substrate between the two adjacent conductive gates (101) and (108).

Allowable Subject Matter

Claims 19, 20, 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with a specific doping concentration for the lightly doped region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
October 19, 2004

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